In-Fab Parameter Characterization for Pinned Photodiodes in CMOS Image Sensors

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***Abstract*—This paper proposes a test methodology that enables early characterization of pinned photodiode (PPD) properties during the CIS fabrication process. The proposed method measures the capacitance of the PPDs simply yet with high precision and facilitates the extraction of key parameters of the PPD. The effectiveness of the proposed method is validated by observing significant changes in these parameters in response to variations in process conditions and the bias voltage of the transfer gate (TG). In addition, the full well capacity (FWC) is successfully extracted from the measured PPD capacitance, consistent with electrical die sorting (EDS) results.**

I. Introduction

THE demand for high-resolution CMOS image sensors has led to a continuous reduction in pixel pitch [1]. However, as pixel sizes shrink, the design complexity of pixel transistors and pinned PPDs increases due to several factors such as charge-transfer characteristics and process-induced variations. Therefore, accurate characterization of key pixel parameters is essential for optimal performance. While transistor characteristics can be readily evaluated during fabrication through test element groups (TEGs), PPD characteristics are typically assessed indirectly from EDS results obtained after chip fabrication. This indirect evaluation makes it difficult to verify PPD characteristics during the manufacturing process, which can negatively impact product development speed and yield control. Furthermore, the lack of direct assessment methods limits the quantitative characterization of PPD parameters, resulting in challenges in process optimization and quality control.

To address these challenges, various attempts have been made. Conventional methods for characterizing PPDs involve using modified pixel structures in TEGs [2] or extraction of parameters from chip-level evaluations [3]. However, the former approaches have limitations because the modified test structures do not accurately reflect the characteristics of the main pixel. The later approach also requires changes to the pixel control circuit and operation timing, which makes them unsuitable for mass production. Moreover, since evaluation is only possible after fabrication and packaging, which makes it difficult to quickly resolve the problems. This paper presents a method based on a TEG structure that enables the direct extraction of key PPD parameters during the CIS fabrication process. The proposed technique allows for precise PPD characterization without requiring full sensor operation making it highly suitable for mass production due to its rapid feedback. By leveraging capacitance-voltage (C-V) measurements and process parameter analysis, this approach provides valuable insights into PPD behavior, facilitating the optimization of CMOS image sensor performance.

II. PPD Characterization Method

Fig. 1(a) shows the proposed TEG schematic, which consists of an array whose unit element includes a PPD, a TG, and a floating diffusion (FD), reflecting the main pixel structure of the chip. The TG, FD, and ground (GND) are connected in parallel, and the array size is chosen to allow for the capacitance measurement with sufficient margin. Fig. 1(b) illustrates the vertical cross-section with the TG switched on and the corresponding energy band diagram, representing the capacitor components measured between FD and GND. C_{PPD} represents the capacitance between the PPD and GND, C_{CH} denotes the channel capacitance of TG, C_{FD} refers to the FD junction capacitance, and C_P accounts for the parasitic capacitance, which include all measured capacitances except for the aforementioned components. The capacitance values of these components vary with FD voltage (V_{FD}), as V_{FD} serves as the reverse bias for the p-n junction. In the energy band diagram, V_{PDMAX} and V_{TGMAX} represent the maximum voltages of the PPD and TG channel regions, respectively. These parameters are crucial because they are related to PPD characteristics such as charge transfer and full well capacity (FWC). The electron energy level, referred to as

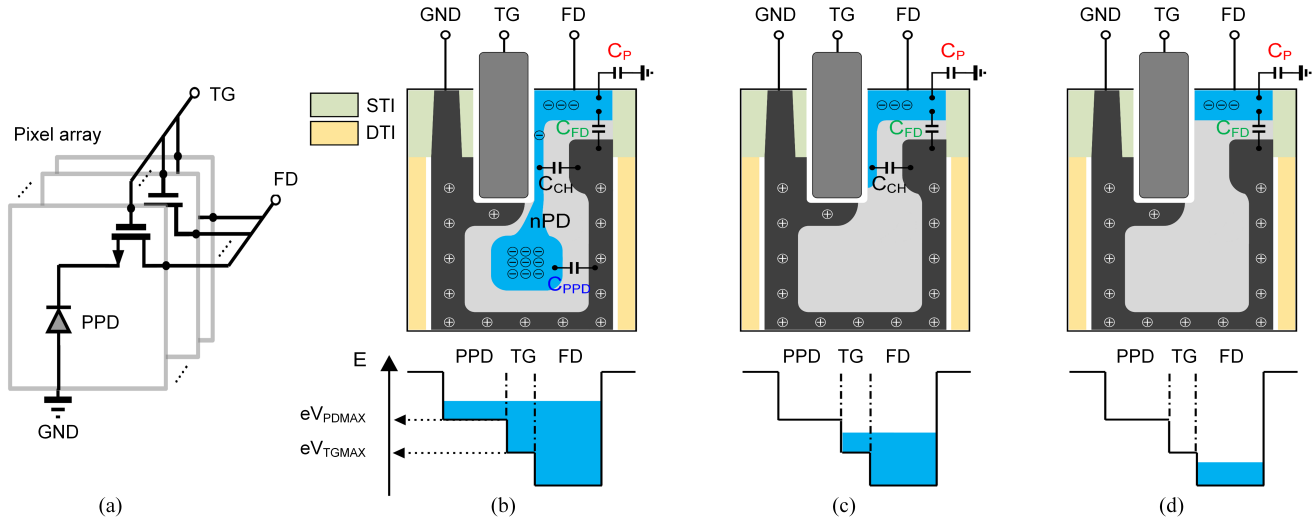

Fig. 1. The proposed TEG structure. (a) Schematic of the TEG. (b)-(d) Vertical cross-sectional structures (top row) and their corresponding energy band diagrams (bottom row), showing the impact of increasing V_{FD} values from (b) to (d).

the water level in the energy band diagram, is determined by V_{FD}. For example, when V_{FD} decreases, this level moves upward. In Fig. 1(b), V_{FD} is set below V_{PDMAX}. As V_{FD} increases, the electron energy decreases, eventually exceeds V_{PDMAX}. Fig. 1(c) shows the case where $V_{PDMAX} < V_{FD} < V_{TGMAX}$. In this case, the PPD is electrically isolated from the FD, so C_{PPD} cannot be measured when measuring the capacitance between FD and GND. Fig. 1(d) shows the case where $V_{FD} > V_{TGMAX}$, where both C_{PPD} and C_{CH} are isolated from the capacitance between FD and GND, resulting in a capacitance of $C_{FD} + C_P$.

Fig. 2(a) and 2(b) show the capacitance between FD and GND when TG is on and off, respectively. By exploiting the capacitance difference, $C_{PPD} + C_{CH}$ can then be obtained, as shown in Fig. 2(c). Fig. 2(d) shows the measured capacitance for TG-on, TG-off, and their difference as a function of V_{FD}. In the high V_{FD} region, the TG-on and TG-off capacitances are equal because C_{PPD} and C_{CH} are isolated from FD in both cases, indicating that V_{FD} exceeds the TG channel potential. As V_{FD} decreases, the point at which the TG-on and TG-off capacitances begin to diverge corresponds to V_{TGMAX}. This indicates that the x-axis intercept of $C_{PPD} + C_{CH}$ represents V_{TGMAX} (inset).

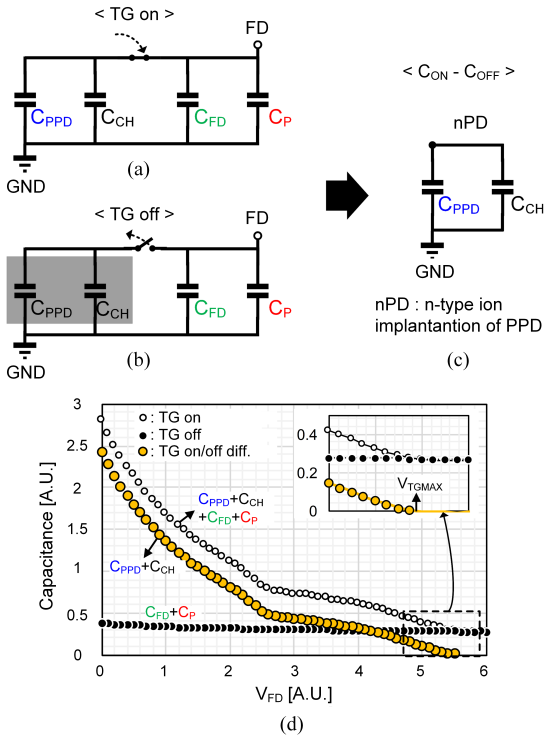

Fig. 2. Capacitance between FD and GND. Capacitance components when (a) TG is on, (b) TG is off. (c) The capacitance difference between TG-on and TG-off corresponds to $C_{PPD} + C_{CH}$. (d) The measured capacitances when TG-on and TG-off, as well as their difference (yellow circles), are plotted as a function of V_{FD}.

Fig. 3 introduces the C_{CH} extraction method from the measured $C_{PPD} + C_{CH}$. Fig. 3(a) describes the vertical structure around the TG, showing capacitance segmentation. C_{TC} and C_{TG} represent the capacitance between the TG gate and the its channel, and the TG gate and GND, respectively. C_{SCR} represents the series connection of C_{TC} and C_{CH}. Fig. 3(b) shows the measured C_{TG} as a function of V_{FD}. In the high V_{FD} region, C_{TG} remains at its maximum value. As V_{FD} decreases, C_{TG} begins to decrease because the TG channel blocks voltage fluctuations when measuring the capacitance between TG and GND, resulting in a capacitance decrease proportional to the TG channel area. This is referred to as the screening effect of

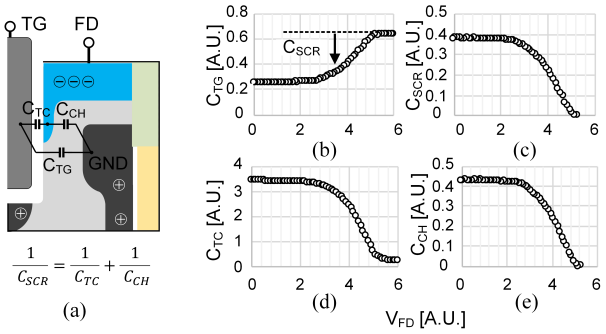

Fig. 3. C_{CH} extraction method. (a) Capacitance segmentation around TG and the measured capacitance as a function of V_{FD} : (b) C_{TG}, (c) C_{SCR}, (d) C_{TC}, and (e) C_{CH}.

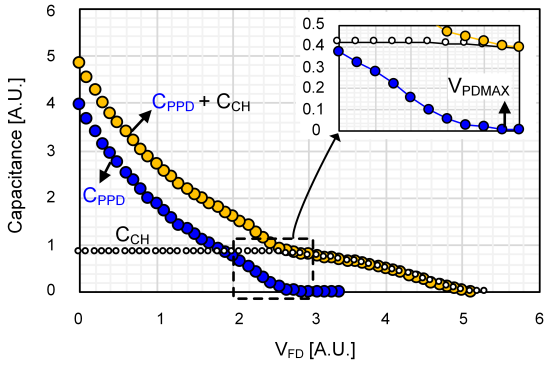

Fig. 4. The proposed PDCV plot, including the measured C_{PPD} (blue circle) and V_{PDMAX} (inset).

the TG channel. The amount of capacitance reduction corresponds to C_{SCR}, as shown in Fig. 3(c). Since C_{TC} is directly measurable (Fig. 3(d)), C_{CH} can be calculated from the C_{SCR} and C_{TC} results, as shown in Fig. 3(e).

Fig. 4, referred to as the photodiode capacitance-voltage (PDCV) plot, shows the measured values of $C_{PPD} + C_{CH}$ and C_{CH} as shown in Fig. 3, as well as their difference, which corresponds to C_{PPD}. Using the same approach as in the extraction of V_{TGMAX}, the point at which the $C_{PPD} + C_{CH}$ and C_{CH} begin to diverge, corresponds to V_{PDMAX}, which also corresponds to the x-axis of the C_{PPD} curve.

III. Measurement Results

The effectiveness of the proposed method is verified by observing the changes in the PDCV plot due to variations in the fabrication process and TG gate bias. Fig. 5 shows the effect of the n-type impurity dose in PPD (nPD). Fig. 5(a) presents the PDCV plot versus nPD dose (increasing from ① to ③). It can be seen that as V_{PDMAX} increases with increasing nPD dose. This is because a higher reverse bias is required to fully deplete the nPD region of the PPD at a higher nPD

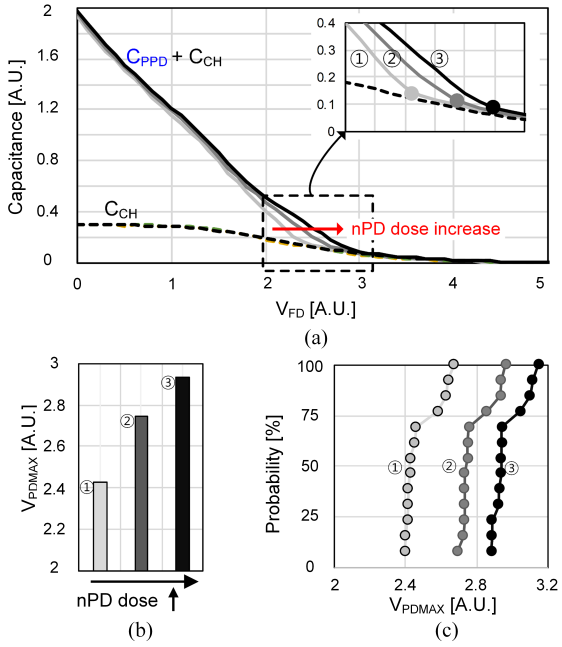

Fig. 5. Effects of nPD IIP dose on V_{PDMAX}. (a) PDCV plots, (b) measured V_{PDMAX}, and (c) in-wafer distribution of V_{PDMAX} with increasing nPD dose. As expected, increasing the nPD dose leads to a corresponding increase in V_{PDMAX}.

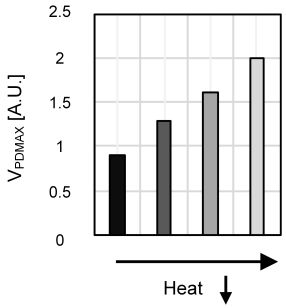

Fig. 6. Effect of process heat on V_{PDMAX}, showing that V_{PDMAX} increases as process heat decreases.

dose. In the low V_{FD} region near 0V, no difference is observed in $C_{PPD} + C_{CH}$. This is because, in this experiment, only the nPD ion implantation process targeted at the depth where V_{PDMAX} is formed is modified among various nPD ion implantation processes. Meanwhile, C_{CH} remains constant across different nPD doses, indicating that nPD ion implantation does not affect the TG channel potential. Fig. 5(b) shows the extracted V_{PDMAX} results from the PDCV plot. Fig. 5(c) shows the cumulative distribution function (CDF) of V_{PDMAX} across the entire wafer. A tailing phenomenon in the CDF corresponds to a specific region on the wafer, demonstrating the method's effectiveness of this method for monitoring process variations within and between wafers.

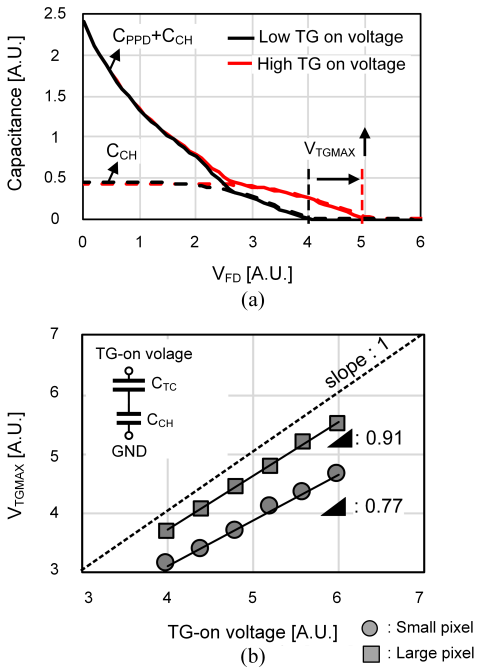

Fig. 7. Effects of TG-on bias voltage on V_{TGMAX}. (a) PDCV plot and (b) V_{TGMAX} as a function of increasing TG-on voltage at different pixel pitches. Pixel with larger pitch exhibits improved short-channel characteristics due to the increased TG gate size.

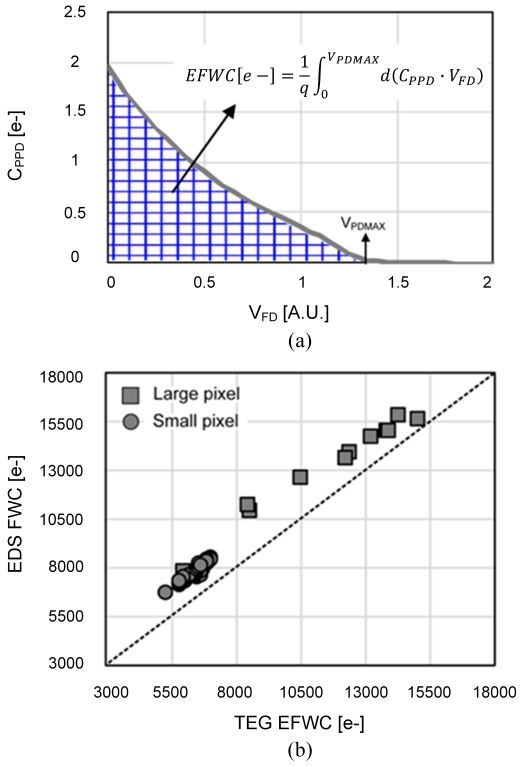

Fig. 8. (a) Estimation of EFWC calculated from C_{PPD}, and (b) comparison of the EFWC with EDS results for different pixel pitches.

Fig. 6 shows the effect of process heat on V_{PDMAX}. As the process heat temperature decreases, the measured V_{PDMAX} value increases. This is because lower temperatures reduce the diffusion of p-type impurities into the nPD region, effectively decreasing the n-type concentration in the nPD region. As a result, a higher reverse bias is required to fully deplete the nPD region, leading to an increase in V_{PDMAX}.

Fig. 7(a) shows a PDCV plot for different TG-on bias voltages, where an increase in V_{TGMAX} is observed at higher TG-on voltages. Similarly, Fig. 7(b) presents the same experiment for small and large pixels. The slope of the TG-on voltage versus V_{TGMAX} reflects the gate controllability, related to the sub-threshold swing of the TG. The measured slopes are 0.91 V/V for large pixel and 0.77 V/V for small pixel, indicating the larger TG has better gate controllability and short-channel characteristics.

Fig. 8(a) shows the measured C_{PPD} curve as a function of V_{FD}. The area under this curve, within the x-axis range from 0 V to V_{PDMAX}, divided by the elementary charge (q), corresponds to the equilibrium FWC (EFWC). Here, "equilibrium" refers to the state when the TG channel voltage is 0 V. Fig. 8(b) compares the EFWC extracted from the TEG with the FWC measured by EDS for different pixel sizes. These two values show a clear correlation with some offset. The offset can be attributed to the fact that the TG channel potential of the main pixel is actually lower than 0 V, while it is assumed to be 0 V when measuring the EFWC.

IV. Conclusion

This paper presents an innovative method to directly extract PPD characteristics during CMOS image sensor fabrication. By using a TEG structure, the method allows precise evaluation of PPD parameters without the need for full sensor operation. This also allows process variations to be instantly identified and corrected. Additionally, the method offers fast, efficient feedback in large-scale production, contributing to the optimization of image sensor performance.

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